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other embodiments electrode may only extend to the upper surface of source region 105. It should also be appreciated that electrode 109 does not separate region 105 into two separate source regions in the illustration of FIG. 5K. Rather, electrode 109 is fabricated in the form of a plug that is sursurounded by N+ material that comprises region 105.

I claim:

1. A method comprising:

forming, in a semiconductor substrate of a first conductivity type, first and second trenches that define a mesa 10 having respective first and second sidewalls;

partially filling each of the trenches with a dielectric material that covers the first and second sidewalls;

filling a remaining portion of the trenches with a conductive material to form first and second field plates in the 15 first and second trenches, respectively, the first and second field plates extending vertically from near a bottom of the mesa to a top surface of the semiconductor substrate:

forming source and body regions in an upper portion of the 20 mesa, the source region being of the first conductivity

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type and the body region being of a second conductivity type opposite to the first conductivity type, the body region separating the source from a lower portion of the mesa, the lower portion of the mesa comprising a drift region, the dielectric material and the field plates being formed with a reduced spacing between the field plates and the mesa near the body region as compared to near the lower portion of the mesa;

forming a gate embedded within the dielectric material adjacent the body region, the gate being insulated from the body region and the fist and second field plates;

forming a drain region of the first conductivity type at the bottom of the mesa, the drain region being connected to the drift region;

forming a source electrode connected to the source region; and

forming a drain electrode connected to the substrate.

2. The method of claim 1 wherein the first conductivity type is n-type.

\* \* \* \* \*